GIET POLYTECHNIC, JAGATPUR, CUTTACK

LESSON PLAN

Discipline: ETC,CSE	Semester: 3rd	Name Of The Teaching Faculty: SUGANDHA PUSPITA MADHUJHARA	
Subject: Digital Electronics(Th-3)	No. Of Days Per Week Class Allotted: 04 P	Semester From Date: 01.07.2024	To Date: 08.11.2024
		No. of weeks: 15	

Week	Class Day	Theory Topic
		UNIT1: BASIC OF DIGITAL ELECTRONICS
1st week	1st	➢ 1.1: Number system: binary, octal, decimal, hexadecimal-conversion from one system to another
	2nd	➢ 1.1: Number system: binary, octal, decimal, hexadecimal-conversion from one system to another
	3rd	➢ 1.2: Arithmetic operation(addition, subtraction, multiplication, division),1's & 2's compliment of binary numbers & subtraction using complement method
	4th	➢ 1.2: Arithmetic operation(addition, subtraction, multiplication, division),1's & 2's compliment of binary numbers & subtraction using complement method
2nd week	1st	➢ 1.3: Digital code & its application and distinguish between weighted and non weighted-code,binary code, excess 3 & gray codes
	2nd	➢ 1.3: Digital code & its application and distinguish between weighted and non weighted-code,binary code, excess 3 & gray codes
	3rd	➢ 1.4: Logic gates(AND,OR,NAND,NOR,EX-OR,EX-NOR)-symbol function,expression,truth table & timing diagram
	4th	➢ 1.4: Logic gates(AND,OR,NAND,NOR,EX-OR,EX-NOR)-symbol function,expression,truth table & timing diagram
3rd week	1st	➢ 1.5: Universal gates & realisation
	2nd	➢ 1.6: Boolean Algebra, Boolean expression, Demorgan's theorems
	3rd	➢ 1.7: Represent logic expression : SOP & POS form
	4th	➢ 1.8: K-map (3 & 4 variables) and minimization of logical expression ,Don't care condition
4th week	1st	**UNIT 2: COMBINATIONAL LOGIC CIRCUIT** ➢ 2.1.1: Half adder, full adder
	2nd	➢ 2.1.2: Half subtractor, full subtractor
	3rd	➢ 2.1.3: Serial & parallel binary 4 bit adder
	4th	➢ 2.1.3: Serial & parallel binary 4 bit adder
5th week	1st	➢ 2.2.1: Multiplexer(4:1)
	2nd	➢ 2.2.2: Demultiplexer(1:4)
	3rd	➢ 2.2.3: DECODER
	4th	➢ 2.2.4: ENCODER
6th week	1st	➢ 2.2.5: Digital comparator(3 bit)
	2nd	➢ 2.3:7 segment decoder(definition, gate level of logic circuit)
	3rd	➢ 2.3: 7 segment decoder(truth table & application)
	4th	➢ 2.3: 7 segment decoder(truth table & application
7th week	1st	**UNIT 3: SEQUENTIAL LOGIC CIRCUIT** ➢ 3.1: Principle of flip flop operation, its types
	2nd	➢ 3.1: Principle of flip flop operation, its types
	3rd	➢ 3.2.1: SR flip flop using NAND
	4th	➢ 3.2..2: SR flip flop using NOR Latch(unclocked)
8th week	1st	➢ 3.2..2: SR flip flop using NOR Latch(unclocked)
	2nd	➢ 3.3.1: Clocked SR flip flop (Logic circuit, truth table & application)

	2nd	➤ Working of Binary-Decimal Encoder & 3 X 8 Decoder
	3rd	➤ Working of Two bit magnitude comparator
	4th	➤ Working of Two bit magnitude comparator
	5th	REVISION
	1st	REVISION
6th week	2nd	➤ **3. SEQUENTIAL LOGIC CIRCUITS** ➤ Give the idea of Sequential logic circuits
	3rd	➤ State the necessity of clock and give the concept of level clocking and edge triggering
	4th	➤ Clocked SR flip flop with preset and clear inputs
	5th	➤ Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
7th week	1st	➤ State the necessity of clock and give the concept of level clocking and edge triggering
	2nd	➤ Clocked SR flip flop with preset and clear inputs
	3rd	➤ Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
	4th	➤ Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
	5th	➤ Concept of race around condition and study of master slave JK flip flop
8th week	1st	➤ Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
	2nd	➤ Give the truth tables of edge triggered D and T flip flops and draw their symbols.
	3rd	➤ Applications of flip flops
	4th	➤ 4-bit asynchronous counter and its timing diagram
	5th	➤ 4-bit asynchronous counter and its timing diagram
9th week	1st	➤ Asynchronous decade counter
	2nd	➤ 4-bit synchronous counter
	3rd	➤ Distinguish between synchronous and asynchronous counters
	4th	➤ State the need for a Register and list the four types of registers
	5th	➤ Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop
10th week	1st	➤ Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop
	2nd	➤ REVISION
	3rd	**8085 MICROPROCESSOR**
	4th	➤ Introduction to Microprocessors, Microcomputers
	5th	➤ Architecture of Intel 8085A Microprocessor and description of each block.
11th week	1st	➤ Pin diagram and description.

	3rd	➢ 3.3.1: Clocked D flip flop (Logic circuit, truth table & application)
8th week	4th	➢ 3.3.1: Clocked JK flip flop (Logic circuit, truth table & application)
	1st	➢ 3.3.1: Clocked T flip flop (Logic circuit, truth table & application)
	2nd	➢ 3.3.1: Clocked JK flip flop (Logic circuit, truth table & application)
9th week	3rd	➢ 3.3.1: Clocked Master slave flip flop (Logic circuit, truth table & application)
	4th	➢ 3.4: Concept of racing and how it can be avoided
	1st	UNIT 4: REGISTERS, MEMORIES & PLD ➢ 4.1.1: Shift register- serial in & serial out, serial in parallel out
10th week	2nd	➢ 4.1.2: Parallel in serial out & parallel in parallel out
	3rd	➢ 4.2: Universal shift registers- applications
	4th	➢ 4.3: Types of counter & application
	1st	➢ 4.4.1: Binary counter , Asynchronous ripple counter(up & down)
	2nd	➢ 4.4.2: Decade counter, synchronous counter, Ring counter
11th week	3rd	➢ 4.5: Concept of memories- RAM, ROM, static RAM, dynamic RAM, PS RAM
	4th	➢ 4.6: Basic concept of PLD & application
	1st	UNIT 5: A/D & D/A CONVERTER ➢ 5.1: Necessity of A/D & D/A converters
12th week	2nd	➢ 5.1: Necessity of A/D & D/A converters
	3rd	➢ 5.2: D/A conversion using weighted resistor methods
	4th	➢ 5.3: D/A conversion using R-2R ladder (Weighted resitors) network
	1st	➢ 5.3: D/A conversion using R-2R ladder (Weighted resitors) network
	2nd	➢ 5.4: A/D conversion using counter method
13th week	3rd	➢ 5.5: Conversion using successive approximate method
	4th	UNIT 6: LOGIC FAMILIES ➢ 6.1: Various logic families & categories according to the IC fabrication process
	1st	➢ 6.1: Various logic families & categories according to the IC fabrication process
	2nd	➢ 6.2.1: Characteristics of Digital ICs- propagation Delay
14th week	3rd	➢ 6.2.2: Characteristics of Digital ICs- fan-out, fan-in, power Dissipation, Noise Margin
	4th	➢ 6.2.3: Characteristics of Digital ICs- power supply requirement & speed with reference to logic families
	1st	➢ 6.3.1: Features, circuit operation & various applications of TTL(NAND)
15th week	2nd	➢ 6.3.1: Features, circuit operation & various applications of CMOS(NAND & NOR)
	3rd	➢ REVISION
	4th	➢ REVISION

29/06/24
Signature of Faculty

29/06/24
Signature of Sr.Lecturer
Head of Dept. (Elec
Electrical & ETC Engg
G. P. T (POLY), ...

29/6/24
Signature of Principal